Report on benchmarking of MOSFET simulations:

Steve Bourland
Mentor: **Michael Duane**

Abstract:

This report summarizes the results of my work at AMD during June 1-August 19, 1998. I installed pdMesh from PDF Solutions, a process-to-device regridding program designed to be used with the Silvaco and Avant! TCAD tools. Following the installation, devices were defined in Silvaco's device simulator Atlas to compare simulation times with and without the pdMesh grid. These devices were also used in a benchmarking study to compare different drift-diffusion mobility models. Drift-diffusion results were also compared against energy-balance and hydrodynamic simulation results. This work is to be included in my Masters thesis. Finally, a PC version of a vendor's TCAD tools was installed during the summer, and a method to run the code remotely on other PC's was established.

1. INTRODUCTION:

Industrial development of device technology today occurs at a rapid pace. The life span of a given device is measured in months. This requires the ability to assess the benefits of new device ideas quickly and accurately. To actually fabricate and test a new device in silicon usually takes a few weeks. Computer simulations allow modified devices to be tested within a few hours, although this can stretch out to days, and also do not consume valuable raw materials or production line time. However, the accuracy of computer models is always subject to question. This has led to the development of many different models for carrier mobility as well as different carrier transport models. Here several different simulation packages were compared on two idealized device structures.

2. GOALS:

The main goal for my work at AMD this summer was to collect data for my Masters thesis. AMD Austin uses the Silvaco TCAD tools which Purdue does not have access to. This allowed me to add Atlas to the list of simulators I could compare. It also provided me with an opportunity to see what industrial fabrication development is like and learn more about simulation and device fabrication issues.

3. ACCOMPLISHMENTS

The first task that was dealt with this summer was the installation of the new pdMesh code from PDF solutions and evaluating its performance. The same structures to be used in my thesis were defined in one of the commercial packages as standard test structures, one with a drawn gate length of 250 nm and the other with a 50 nm gate. In order to use pdMesh with the 50 nm device, a new control script had to be written for such a small scale structure with the help of PDF Solutions. It was found that using the pdMesh defined grid cut the simulation time by over 30% on average with less than 1% change in drain current results in all cases.

After collecting the drift-diffusion model data, the advanced transport models in this package were tested. Both hydrodynamic and energy balance models are offered, although only the energy balance model is suggested for use by the vendor. The difference between the hydrodynamic and energy balance models in this package is that the energy balance model has a strong carrier temperature dependence in the carrier mobility, while the hydrodynamic model allows much higher mobilities with increased carrier temperature. The hydrodynamic model demonstrated much better convergence behavior versus the energy balance model. The hydrodynamic simulations consistently took over four times as long to run as the drift-diffusion simulations and did not provide results consistent with those from other hydrodynamic models (e.g. UT-Minimos). The drain current for the 50 nm device increased by less than 10% when using this hydrodynamic model instead of the drift-diffusion model, while other hydrodynamic codes have shown differences of almost 50%. Although 50% may be

too much of an increase to be realistic, at this dimension, advanced transport models should report noticeably higher on-currents. Given the small difference in drain current results from the hydrodynamic simulations and the difficulties converging with the energy balance model, it was decided that the advanced transport models were not worth the effort to use with this code.

Perhaps the most personally rewarding experience from my summer in Austin was being a co-inventor on a patent application that is being filed. This patent is for an advance transistor structure that will hopefully provide both increased chip speed and reduced power dissipation in the future.

4. CONCLUSIONS:

Having never worked with a regridding program before, I was very impressed with the efficiency of the grids generated by the pdMesh program. Although it does take quite a bit of time to get a good control script to drive the program, once that is done the script can be used on any device that is of similar dimension. This then offers at least a 30% timesaving on each simulation, which can quickly make up for the time invested to define the control script.

In the benchmarking study of many different drift-diffusion mobility models in several different software packages, it was found that the drift-diffusion default parameter models had on-current spreads of approximately 10% for the 250 nm device, but the spread increased to 30% for the 50 nm device. The fact that mobility models had a strong influence on the current for the 50 nm device demonstrates that mobility continues to be an important parameter even under conditions of heavy velocity saturation.

A comparison was also made between the Lombardi and Universal mobility models in a commercially available package with parameter sets which model AMD's production 250 nm device well (see figures 1 and 2). These models predicted on-currents within 5% of each other on the idealized 250 nm device used in this work. However, these models had differences of almost 15% for the 50 nm device. This demonstrates that models calibrated to one technology need to be re-evaluated when used with another technology since models scale differently.

Comparing the "calibrated" parameter set against the default Lombardi model within this package demonstrates a 15% difference for the 250 nm device, but over 30% with the 50 nm device. This suggests that even at these small dimensions, adjustments to the parameters in the mobility model still have a strong affect on the predicted drain currents.

A comparison was made between allegedly identical mobility models in different simulation packages. Using the Lombardi mobility model, one package predicted 20% more drain current than another for the 250 nm device. But for the 50 nm device, the first package predicted 5% less drain current than the second (see figures 3 and 4). In another comparison, using the University of Texas mobility model, UT-Minimos predicted 10% more current than commercial package A for the 250 nm device, but only 5% more for the 50 nm device (see figures 5 and 6). This suggests that the differences caused by different solution methods are less pronounced as devices shrink, although these differences are still under investigation. With the complexity of this simulation packages, ensuring that the same problem is being solved in two different programs is always subject to question.

What I consider to be the most important finding of my work is that simulated drain currents will continue to be very sensitive to the mobility model even as devices scale to L = 50 nm. Seeing this in drift-diffusion simulations is quite surprising, since there is strong velocity saturation for such short channels. I expect hydrodynamic or energy transport models to be more sensitive to the mobility models. Another key observation is that mobility models that agree fairly well at L = 250 nm scale differently to 50 nm where normal electric fields and channel doping concentrations are higher. Given the continued importance of mobility and the known normal field and doping concentration limitations of current mobility models, it would be beneficial for AMD to help in the development of new models. In this regard, the recent work by the Bell Labs group (M.N. Darwish, et al, "An improved electron and hole mobility model for general purpose device

simulation," *IEEE Transactions on Electron Devices*, vol. 44, pp. 1529-1538, 1997) may be worth considering.

5. ACKNOWLEDGEMENTS:

I would like to thank everyone in the integration group for their encouragement and willingness to answer my endless stream of questions. I would also like to express my gratitude to Lori MacKinnon for helping me "get things done," and Carl Huster for providing me with mobility model parameter sets. Finally, I would like to thank Dani Kadosh and my mentor Michael Duane for giving me the opportunity to see device development from a new perspective.

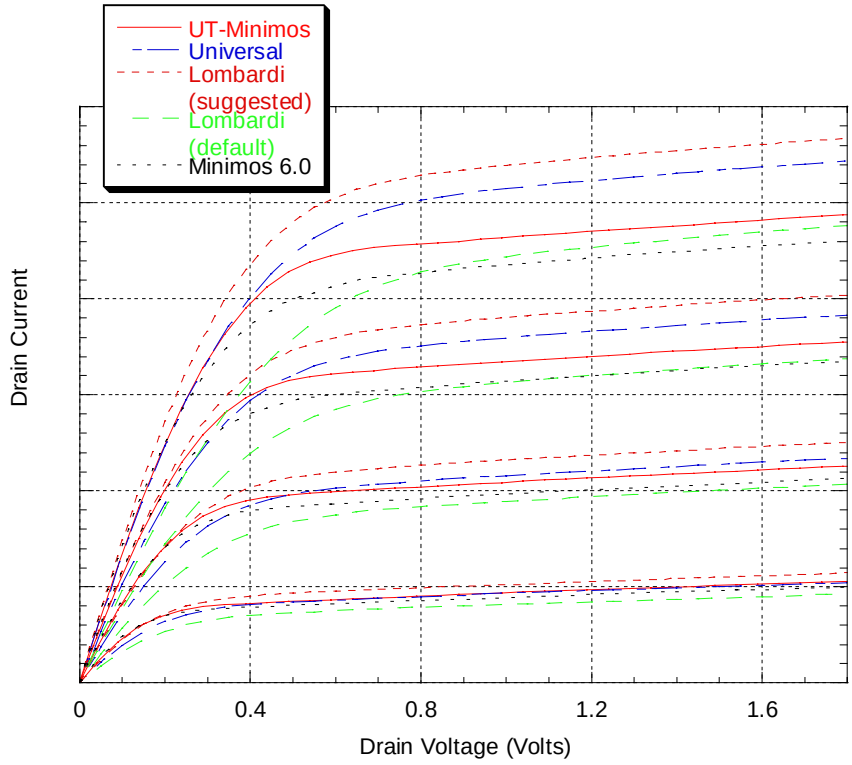

Fig. 1 Drain current versus drain voltage for the 250 nm device

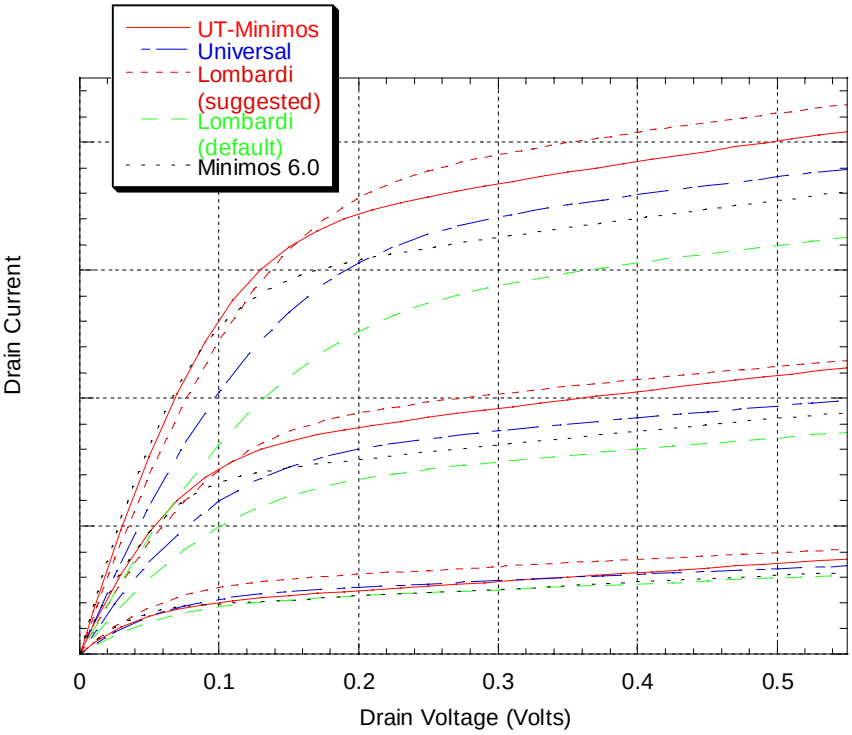

Fig. 2 Drain current versus drain voltage for the 50 nm device

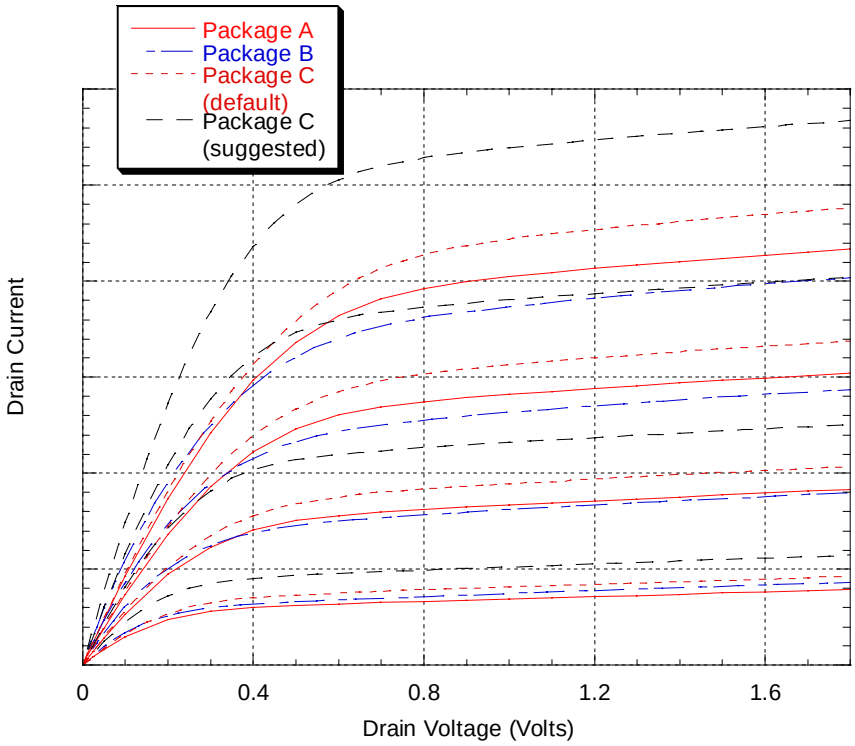

Fig. 3 Drain current versus drain voltage for the 250 nm device using the Lombardi mobility model

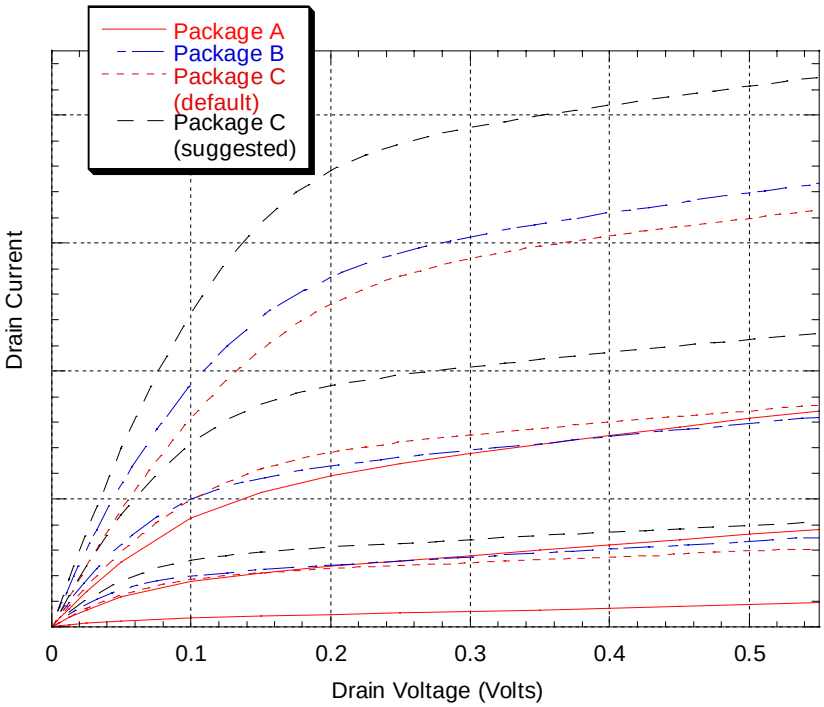

Fig. 4 Drain current versus drain voltage for the 50 nm device using the Lombardi mobility model.

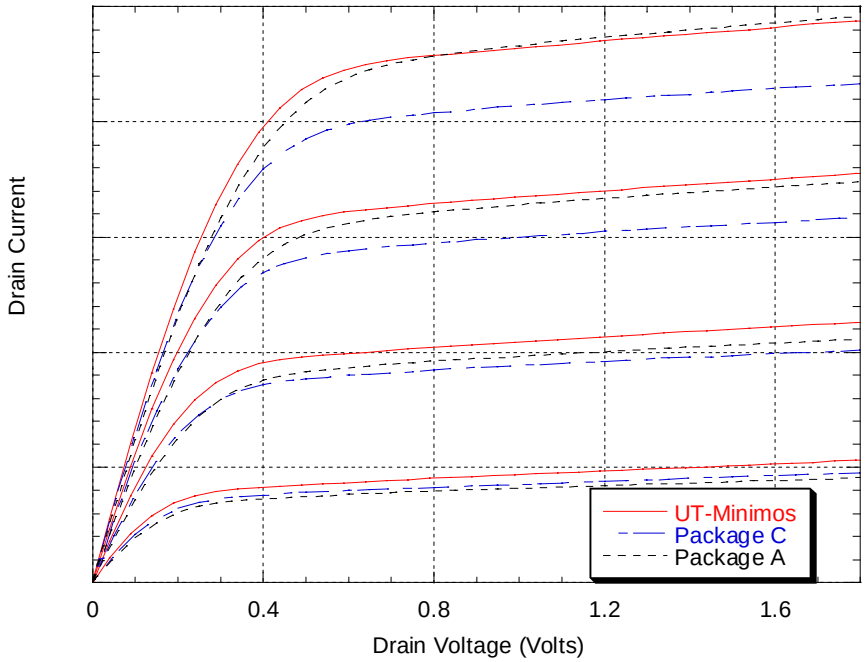

Fig. 5 Drain current versus drain voltage for the 250 nm device using the Arora/Texas mobility models

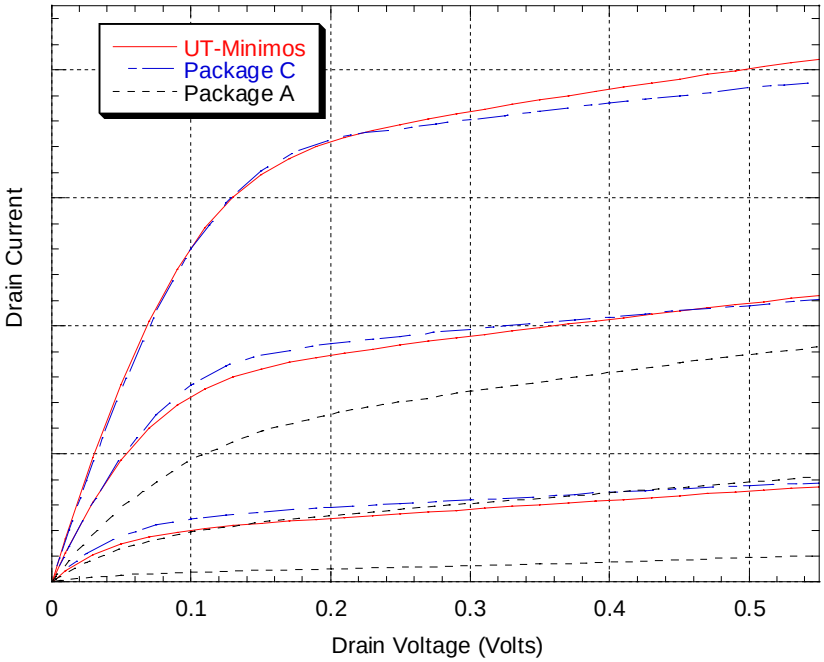

Fig. 6 Drain current versus drain voltage for the 50 nm device using the Arora/Texas mobility models